Total ionizing dose effect modeling method for CMOS digital integrated circuit*

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Simulating the total ionizing dose (TID) of an electrical system using transistor-level models can be difficult and expensive, particularly for digital integrated circuits (ICs). In this study, a method for modeling TID effects in complementary metal-oxide semiconductor (CMOS) digital ICs based on the input/output buffer information specification (IBIS) was proposed. The digital IC was first divided into three parts based on its internal structure: the input buffer, output buffer, and functional area. Each of these three parts was separately modeled. Using the IBIS model, the transistor V-I characteristic curves of the buffers were processed, and the physical parameters were extracted and modeled using VHDL-AMS. In the functional area, logic functions were modeled in VHDL according to the data sheet. A golden digital IC model was developed by combining the input buffer, output buffer, and functional area models. Furthermore, the golden ratio was reconstructed based on TID experimental data, enabling the assessment of TID effects on the threshold voltage, carrier mobility, and time series of the digital IC. TID experiments were conducted using a CMOS noninverting multiplexer, NC7SZ157, and the results were compared with the simulation results, which showed that the relative errors were less than 2% at each dose point. This confirms the practicality and accuracy of the proposed modeling method. The TID effect model for digital ICs developed using this modeling technique includes both the logical function of the IC and changes in electrical properties and functional degradation impacted by TID, which has potential applications in the design of radiation-hardening tolerance in digital ICs.

Keywords: CMOS digital-integrated circuit, Total ionizing dose, IBIS model, Behavior-physical hybrid model, Physical parameters

I. INTRODUCTION

Many cosmic rays with different energy ranges exist in the Universe. Cosmic ray particles include protons, neutrons, electrons, charged particles, photons, and other types of particles, with energies in the Mega to Exa-volt range. The electrical characteristics of the electronic components exposed to radiation are disturbed and degraded.

Among the different radiation effects, the total ionizing dose (TID) effect impacts the electrical characteristics of MOSFETs, generating changes in the transconductance, leakage current, and threshold voltage drift. This is a cumulative effect that cannot be avoided in orbit but is the principal factor influencing the service life of electrical components. Because spacecrafts contain a significant number of MOSFETs and the TID effect is widespread in low Earth orbit (LEO), medium Earth orbit (MEO), geosynchronous Earth orbit (GEO), and deep-space exploration environments, the damage to MOSFET performance caused by the TID effect must be evaluated.

Currently, methods for evaluating the TID effect of electronic components primarily include experiments and model simulations. The former is dependent on the instrumentation environment and is costly, whereas the latter is a quick and inexpensive primary approach to assess the irradiation damage of a component.

Several significant advances in the research on the impact of TIDs on MOSFETs have been made in computer science, ICs, and semiconductor technologies. References [1–9] studied the impact of TIDs on MOS components using semiconductor physics and technology computer-aided design (TCAD) software simulations. The impact of the TID on the threshold voltage of the MOS components was studied in [10–13]. According to the findings, The TID mainly impacts the threshold voltage drift caused by the interface- and hole-trap charges formed in the oxide layer, as well as the increase in leakage current and decrease in carrier mobility. To model the TID effect, references [14–17] developed a model of MOSFET deterioration triggered by the TID effect, and references [18–25] produced a numerical model of the TID effect and analyzed its I-V curve. Owing to the rapid advancement in artificial intelligence, Jia et al. [26] applied neural networks to capture the electrical characteristics of transistors and developed a unique transistor model with more accurate DC characteristics than traditional models. SPICE models of the TID and damage effects of MOSFETs were developed using the macroscopic modeling approach references [27, 28], and the simulation results confirmed the combined influence of the subsequent results in the advanced degradation of MOSFET characteristics and CMOS circuits.

Because of the high computational costs and limited circuit size for simulations, recent modeling and simulation approaches are not suitable for large-scale digital ICs. In this study, a method for modeling the TID effect of CMOS digital ICs is proposed based on the input/output buffer information specification (IBIS) model. This is a hybrid behavioral and physical level model that accurately represents both the logic functions of the digital components and physical parameters of the TID effect on the component ports. This is achieved using the VHDL-AMS language, which enables faster simulations of the TID effect on large digital ICs, compared to transistor-level modeling [29].

* Supported by the special fund of the State Key Laboratory of Intense Pulsed Radiation Simulation and Effect (No.:SKLIPR2011)

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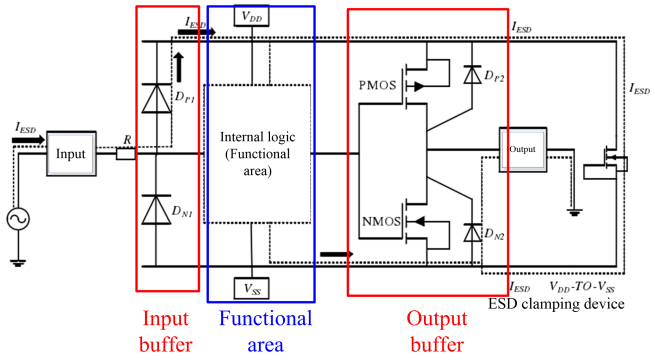
II. METHODOLOGY

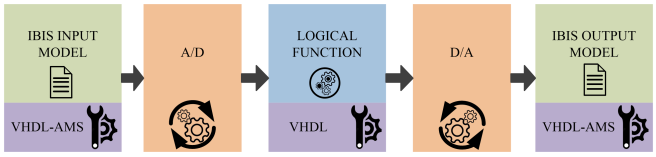
The IBIS model is a file format used to describe various input and output buffer characteristics of a component [30]. An IBIS file is composed of three core parts: file header, component description, and model description, all of which provide data to effectively identify all the input, output, and I/O-type buffers of a device. The file header includes information, such as the IBIS version, file name, and other critical information. The component description includes package parameters, pin mappings, component names, and other key information. Finally, the model description provides the buffer type, threshold level, and four different types of V-I data tables: pullup, pulldown, power clamp, and GND clamp. Moreover, it includes V-T data tables showing the rising and falling edges of the buffer state changes. This format combines radiation electronics and signal transmission information to accurately describe the behavior of component buffers.

A. Overview of the Method

The internal structures of the digital components are shown in Fig. 1(a), where an input signal from outside the component first passes through the internal logic circuit through the input buffer and is transmitted to the external circuit through the output buffer after passing through the internal logic circuit. Properly expressing the actual input–output connection of a component requires an accurate description of both the internal logic and electrical properties of the input–output buffer.



(a)



(b)

Fig. 1. Diagram of the (a) internal structure of a digital component and (b) equivalent hybrid behavioral—physical model.

Consequently, we attempted to match Fig. 1(a) to the hybrid behavioral-physical model structure of the CMOS digital IC, as shown in Fig. 1(b). In this hybrid model, the CMOS digital IC is separated into three parts: input buffer, functional region, and output buffer; the functional region describes the logic function of a digital integrated circuit and is modeled using VHDL language using component Boolean expressions and data from the datasheet. The input and output buffers provide the physical characteristics of the digital IC ports, which are modeled using VHDL-AMS for the port-transistor physical properties of the digital IC.

The input and output buffers of a CMOS digital IC are both equipped with electrostatic discharge (ESD) protection circuits, which typically consist of clamp diodes and ground-gate NMOS (GGNMOS) components. Diodes are extensively used in low-voltage ESDs. The input buffer includes an ESD protection circuit with upper- and lower-clamp diodes D_{P1} and D_{N1}, respectively, as shown in Fig. 1(a). These diodes were physically reconstructed using an a reference approach identical to the one that was used to model the output buffer based on the electrical characteristic curves of the clamp diodes derived from the IBIS model data. The hybrid model perfectly satisfies our demand for modeling the TID effect of a CMOS digital IC because it can operate effectively at various voltages without any operating point limitations and can integrate the TID effect model of a MOSFET.

I/O-port circuits are more sensitive to TID effects than core circuits. This is because I/O-port circuits typically include components such as input buffers and output drivers, which are often designed with small dimensions and thin-film structures, making them more susceptible to radiation. Additionally, A large contact area and concentration of electric fields between the port circuits and external devices further increase the probability of radiation-induced ionization effects.

Therefore, this study focuses on the TID effect on the input/output ports of a component. The aim of this study is to estimate the degradation of the electrical characteristics of the output port caused by the TID effect. This is achieved by applying a hybrid model that considers the TID effect of MOSFETs with ports.

Fig. 2 shows the modeling method of the TID effect for digital components based on the IBIS model, which can be divided into three phases: Modeling the golden effect, modeling the TID effect, and simulation and analysis. The details of each phase are as follows:

(1) Modeling of the golden. This phase is divided into three sub-phases. The input buffer data within the IBIS model of the digital device were preprocessed in the first sub-phase to produce characteristic curve data that represent the V-I characteristics of the diodes in the input buffer. Subsequently, the physical characteristic parameters of the diodes in the input buffer were extracted using their physical equations. The output buffer data within the IBIS model of the digital component were processed in the second sub-phase to generate characteristic curve data that represented the V-I characteristics of the transistors in the output buffer. The physical characteristic parameters of the transistors in the output buffer were extracted using their physical equations.

After the first and second subphases, the specific parameter values of the diodes and transistors in the I/O buffer can be

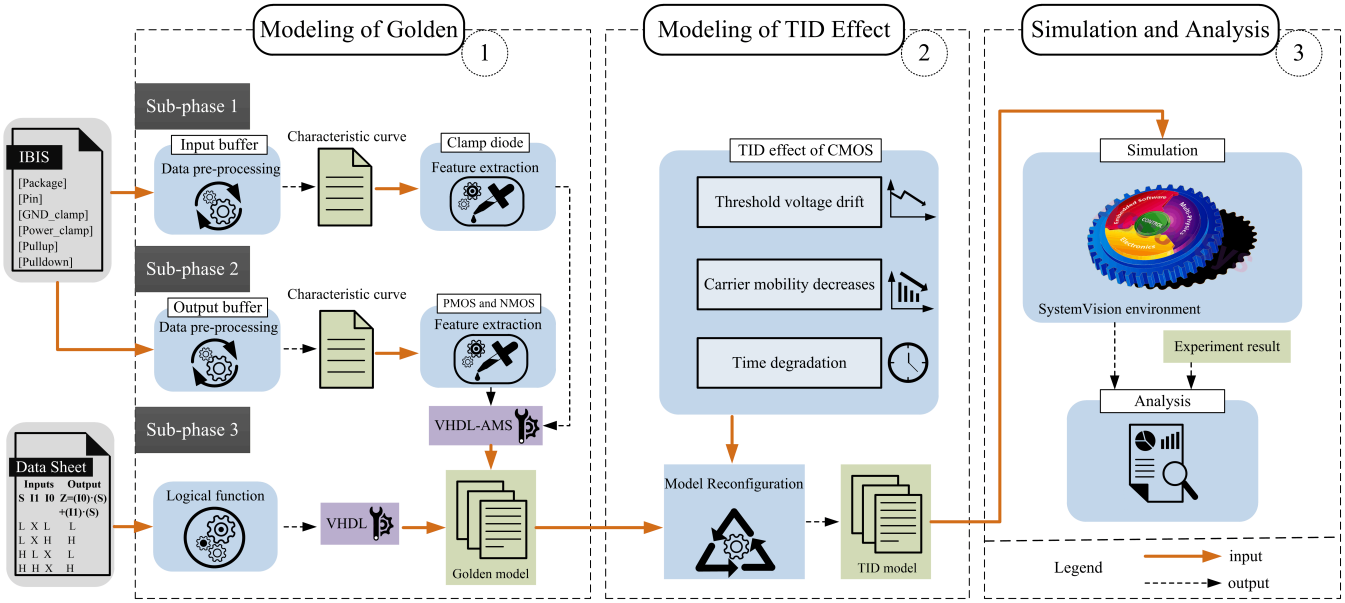


Fig. 2. Process of modeling method of TID effect for digital component.

obtained. The characteristic parameters were then described as input and output buffer models using VHDL-AMS. Based on the datasheet of the digital component, the logical function of the component is described as a functional model in the third subphase using VHDL.

By the end of the first phase, the three previously mentioned models were integrated into the golden model of the digital component, which is based on the input and output buffer models, as well as the functional model. The resulting model takes the form of an executable program file that can implement the behavioral function of the digital component while also reflecting the physical characteristics of the ports.

The delay information in the golden model was obtained by consulting the device data sheet.

(2) Modeling of the TID Effect. The second phase of the proposed TID effect-modeling method is the reconstruction of the golden model generated in the first phase. In this phase, TID variables are added to the golden model based on the influence of TID effects on CMOS digital components, including threshold voltage drift, carrier mobility degradation, and timing degradation, to describe the impact of the TID on CMOS digital components and create an entire TID effect model of the digital component.

The threshold voltage and carrier mobility for the TID effect were extracted from the measured V-I curves, whereas the delay information for the TID effect was obtained from the measured V-T curves.

(3) Simulation and Analysis. Simulation and comparative analysis of the TID model constituted the third phase. In this phase, the TID model was loaded into the simulation environment SystemVision, and the simulation results were generated. The simulation results were then compared with the experimental results, and the accuracy of the modeled results and feasibility of the proposed method were verified.

B. Data Pre-Processing and Feature Extraction

1. *Characteristic Curve of the Clamp Diode at the Input Port*

The power-clamp data within the IBIS model describe the voltage–current relationship of the input port when input voltage V_{in} surpasses the component supply voltage *VCC*. During this period, as shown in Fig. 3(a), the input port ground-clamp diode reverses the cutoff, whereas the power supply clamps the positive conduction of the diode.

Given that the reverse current of the diode is significantly smaller than its forward conduction current and that the input buffer inverter-gate leakage current is negligible, it can be assumed that this dataset corresponds to the V-I characteristic curve of the power-supply clamp diode. Notably, the IBIS model indicates that voltage V_{table} within the power-clamp data table adheres to the following relationship:

$$V_{table} = VCC - V_{in}, \tag{1}$$

where *VCC* is the power supply voltage and V_{in} is the voltage of the input pin. When analyzing the V-I characteristics of a power supply clamp diode, the corresponding voltage V should be obtained using the following transformation:

$$V = V_{in} - VCC = -V_{table}, \tag{2}$$

Similarly, the GND Clamp refers to the voltage of the input pins and current characteristics when the input voltage is below the GND level. During this moment, the power-clamp diode reverses, and the ground-clamp diode conducts positively (Fig. 3(b)). Consequently, the GND Clamp data represent the V–I characteristic curve of the ground-clamp diode.

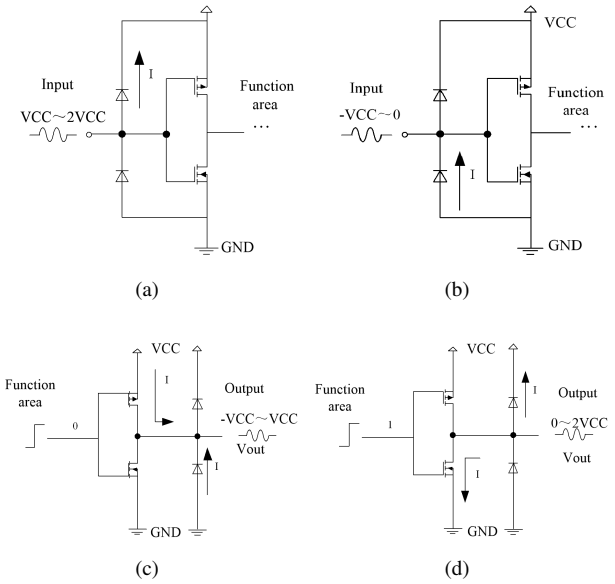


Fig. 3. Schematic of the V-I characteristic curve extraction of the component for the (a) power Clamp, (b) GND clamp, (c) pullup, and (d) pulldown.

Voltage V_{table} in the GND Clamp data table has the following relationship according to the IBIS model:

$$V_{table} = V_{in} - V_{GND}, \tag{3}$$

where V_{GND} is the voltage of the ground; thus, to extract the V-I characteristics of the ground-clamp diode, voltage *V* must be obtained using the following transformation:

$$V = V_{GND} - V_{in} = -V_{table}, \tag{4}$$

2. *Characteristic Curve of the Transistor at the Output port*

The driver inverter and ESD-protection circuit are the major components of the output port of the digital component. Different types of output buffers exist, such as push–pull, I/O, and open-drain buffers. Each buffer type has a different circuit structure and function. Consequently, the V-I curves for the different buffer types differ; an illustration of the fundamental push–pull output is presented along with an explanation of methods to extract the transistor characteristic curve for the port circuit. Notably, this extraction approach is also applicable to other buffer types with minor modifications, as required.

The pullup curve shows the voltage–current relationship of a pin when the output state was set at one. The pull-up PMOS is enabled at this time, whereas the pulldown NMOS is disabled. A scan voltage in the range of *-VCC* to 2 *VCC* was applied to the output pin to obtain the voltage–current relationship. According to the IBIS model, voltage V_{table}, described in the pullup datasheet, is defined as

$$V_{table} = VCC - V_{out}. \tag{5}$$

To extract the output characteristics of the pullup PMOS, the V-I data must be obtained inside the *-VCC* to *VCC* range of the output pin voltage $Vout$, which corresponds to the 2 *VCC* to 0 V interval of the pullup curve. Fig. 3(c) shows the state of the output port during this period.

In addition, the IBIS output-buffer model pulldown data can be used to determine the pulldown curves of NMOS and power-clamp diodes. The pulldown curves show the relationship between the voltage and current of the pin when the output state is set at zero. During this period, the pullup PMOS was disabled, and the pulldown NMOS was enabled. Subsequently, scan voltages ranging from *-VCC* to 2 *VCC* were applied to the output pin. The voltage–current relationship was determined for the output pin. The data between 0 and 2 *VCC* is captured on the Pulldown curve. The voltage and current at the output pin were observed at this stage, as shown in Fig. 3(d).

C. Feature Extraction

1. *Extract Model Parameters of Clamp Diode*

In the previous section, we discussed a method for obtaining the electrical characteristics of transistors using the IBIS model. The following section focuses on the method for selecting a suitable physical model of the transistor for parameter extraction.

The model equation for a diode based on semiconductor physics [31] can be expressed as follows:

$$I_D = I_s(e^{\frac{V_D}{nV_T}} - 1), \tag{6}$$

where I_s represents the reverse-saturation current with a typical value ranging from 10×10^{-6} A to 20×10^{-6} A; V_D is the junction voltage, which equals the diode terminal voltage minus the parasitic resistance drop; V_T is the thermal voltage constant with a typical value of 25.8 mV at 25 °C; and *n* represents the emission coefficient.

The reverse-saturation current I_s, emission coefficient *n*, and parasitic resistance *R* govern the DC behavior of a diode. Modeling only the essential parameters while leaving the other parameters at their default values is acceptable.

To obtain the values of the parasitic resistance *R*, emission coefficient *n*, and reverse-saturation current I_s, reference point coordinates were first selected from the forward characteristic curve of the diode. These coordinates were substituted into Eq. (6), to determine the parameter values.

In this study, a classic digital component CMOS noninverting multiplexer, NC7SZ157, was used as an example to demonstrate the modeling process. The golden parameter values of the diode for NC7SZ157 were obtained, as listed in Table 1, using the diode characteristic parameter-extraction technique along with a datasheet search. These values were

TABLE 1. Golden model parameters of the input port.

Parameter Description	Model Parameters	Values
Package capacitance C_comp	Capacitance *C*	2 *pF*
Pin parasitic resistance R_pkg	Resistance *R*	32 $m\Omega$
Pin parasitic inductance L_pkg	Inductance *L*	1.01 *nH*
Pin parasitic capacitance C_pkg	Capacitance *C*	0.13 *pF*
	Reverse saturation current I_s	2.18× 10^{-28} *A*
Ground clamp diode	Emission factor *n*	1
	Parasitic resistance *R*	1.14 Ω

established as a part of this study. Notably, when analyzing the IBIS model of NC7SZ157, the power-clamp diode was not included. Therefore, only the ground-clamp diodes are listed in Table 1. The input model parameters for the TID effect were extracted using the same method based on measured IBIS experimental data.

2. *Extract Model Parameters of a MOSFET*

(i) Threshold Voltage V_{th}

The threshold voltage is the turning point for the formation of the inverse layer of the MOS component, and a conduction channel is formed when the gate voltage is greater than the threshold voltage. Numerous methods for extracting the MOSFET threshold voltage exist, such as the line extraction, constant current, leakage current second-order derivative, transconductance extraction, Y-function, and beta-function methods [32, 33]. In this study, the linear extrapolation method was chosen for threshold voltage extraction because of its suitability for components with different channel lengths and its potential to make full use of the transistor output characteristics.

The linear extrapolation method is based on the principle that when V_{ds} is small, the MOSFET output characteristics can be expressed as

$$I_{ds} = \frac{W\mu_n C_{ox}}{L}(V_{gs} - V_{th})V_{ds}, \tag{7}$$

where *W* is the gate width, μ_n is the carrier mobility, C_{ox} is the capacitance of the gate-oxide unit area, and *L* is the gate length. For a given V_{ds} drain current I_{ds} depends linearly on gate voltage V_{gs}. The straight line with the steepest slope can be identified by extrapolating the component transfer characteristics. The intersection of this line with the horizontal axis (V_{gs}) indicates the threshold voltage. The reason for choosing the point with the maximum slope is that the subthreshold current dominates the curve when V_{gs} is small, whereas the carrier mobility decreases with increasing gate voltage when V_{gs} is large.

(ii) Saturation Voltage V_{sat}, Saturation Current I_{sat}, Conductance Parameter K_n and Channel-length Modulation Coefficient V_A

When the MOSFET operates in the linear region, the relationship between the drain voltage and the current is as follows [10]:

$$I_{ds} = \frac{W\mu_n C_{ox}}{2L}(2(V_{gs} - V_{th}) - A_{bulk}V_{ds})\frac{V_{ds}}{1 + \frac{V_{ds}}{LE_c}}, \tag{8}$$

where A_{bulk} is the body charge effect coefficient and E_c is the critical electric field for velocity saturation.

To extract the values of the saturation voltage V_{sat}, saturation current I_{sat}, Conductance Parameter K_n, and channel-length modulation coefficient V_A, the reference point coordinates are selected from the linear region of the output characteristic curve of the MOS transistor. These coordinates were substituted into Eq. (8) to obtain parameter values.

Consequently, the parameters associated with the short-channel model of the MOSFET were successfully extracted. The extracted NC7SZ157 output buffer golden model parameters are listed in Table 2 (V_{gs} = 3.3V). The output model parameters for TID effect were extracted using the same method, based on the measured IBIS experimental data.

D. Modeling the TID Effect of a CMOS Digital IC

1. *Effect of Ionizing Radiation on the Electrical Properties of MOS Components*

The TID effect causes two types of charge traps to form within the oxide of the MOS components [34, 37]: fixed oxide charge (*Not*) and interface-trapped charge (*Nit*). These charges are responsible for changes in the electrical behavior of the components, resulting in a number of events, such as threshold voltage drift and carrier mobility degradation.

According to recent studies, the threshold voltages of NMOS and PMOS tend to decrease with increasing TID. However, NMOS exhibits a rebound effect at higher doses [35]. In addition, the TID effect results in a decrease in the carrier mobility of the MOS device and, hence, a decrease in transconductance. Because of the profound effect of carrier mobility attenuation on the MOS device transconductance and current-handling capability, this effect requires careful consideration when analyzing the TID effects of MOS devices [36, 37].

Changes in the threshold voltage and carrier mobility can affect the conduction resistance of the transistor at the output of the component, increasing the conversion time. This

TABLE 2. Golden model parameters of output port .

Parameter Description	Model Parameters	Values
Package capacitance C_comp	Capacitance *C*	1.25 *pF*
Pin parasitic resistance R_pkg	Resistance *R*	32 $m\Omega$
Pin parasitic inductance L_pkg	Inductance *L*	0.91 *nH*
Pin parasitic capacitance C_pkg	Capacitance *C*	0.13 *pF*
Ground clamp diode	Reverse saturation current I_s	5.918×10^{-14} *A*
	Emission factor *n*	1.14
	Parasitic resistance *R*	0.2158 Ω
Power clamp diode	Reverse saturation current I_s	6.59×10^{-11} *A*
	Emission factor *n*	2
	Parasitic resistance *R*	21 Ω
Pulldown NMOS	Threshold voltage V_{th}	0.5V
	Speed saturation potential *B*	5.5 *V*
	Conductivity parameter K_n	$0.02191\Omega^{-1}$
	Groove length modulation factor V_A	40.66 *V*
	Volume charge effect coefficient A_{bulk}	1.2
Pullup PMOS	Threshold voltage V_{th}	-0.6 *V*
	Speed saturation potential *B*	-20 *V*
	Conductivity parameter K_n	$0.01496\Omega^{-1}$
	Groove length modulation factor V_A	-11.62 *V*
	Volume charge effect coefficient A_{bulk}	1.2

occurs during a rising-edge transition when the NMOS transistor is gradually turned off and the PMOS transistor is gradually turned on. The conversion time of the waveform is related to the conduction resistance of the PMOS transistor and size of the load capacitor. The TID effect causes a negative drift in the threshold voltage of the PMOS and a decrease in the channel carrier mobility, that is, an increase in the on-state resistance, which leads to an increase in the time constant of the RC circuit formed by this equivalent resistance, port parasitic or load capacitance, and a longer rise time. During a falling-edge transition, the PMOS transistor gradually turns off, the NMOS transistor gradually turns on, and the parasitic or load capacitance is discharged through the NMOS transistor. TID irradiation can cause both the threshold voltage and carrier mobility of the NMOS transistor to decrease, and because the effect of the two on the conduction resistance is opposite, their mutual canceling effect results in a less pronounced change in the falling-edge waveform compared to the PMOS transistor with varying TID.

2. *Behavior–Physical Hybrid Model of CMOS Digital IC*

In this study, a CMOS noninverting multiplexer, NC7SZ157, was used as a case study to illustrate the process of creating a hybrid model, as shown in Fig. 1(b) and Fig. 2. The gold functional area, input buffer, and output buffer models of NC7SZ157 were developed as the first steps of this process.

(i) Modeling of Functional Area

The functional domain of the behavioral-physical model of the hybrid digital IC pertains to the description of the logic function of the component being investigated along with its digital behavior. The complexity of this module varies, depending on the function and size of the device being studied. Constructing the model as a separate and callable module facilitates ease of readability and future modifications, which is highly recommended.To illustrate the efficacy of this concept, the paper employed the NC7SZ157 datasheet to describe the functional area in VHDL, as indicated in Alg. 1. The input ports in Alg. 1 are denoted as *S*, *I0*, and *I1*, respectively. In contrast, *Z* denotes the output port of NC7SZ157.

Algorithm 1: Behavior model of functional for NC7SZ157

1 Define an entity called ”multiplexer,” which has inputs *S*, *I1* and *I0*, and output *Z* of type std_logic
2 End-entity header
3 Begin the architecture ”behav” for the entity ”multiplexer”
4 Beginning a process sensitive to changes in the signals *S*, *I1*, and *I0*
5 If the value of signal *S* equals a high-level ’1, then Assign the value of the signal *I1* to the output *Z*. If the value of the signal *S* equals the low level ’0, then Assign the value of the signal *I0* to the output *Z*
6 End the process
7 End the architecture

(ii) Modeling of Input Port

Based on the model parameters in Table 1, a physical model of the input port for the NC7SZ157 was designed using VHDL-AMS, as shown in Alg. 2.

Algorithm 2: Physical model of input port for NC7SZ157

We define the electrical terminals VCC, P_in, n1, n2, and out,
Instantiate an entity called "VDC" with the name VDC
Set generic parameters for VDC1 : DC = 3.3
Connect VDC1 to VCC (Electrical _ref
Instantiate an entity called "Diode" with the name Diode1
Set generic parameters for Diode1 : Isat = 2.18E-28, R = 1.14, n = 1.0
Connect Diode1 to electrical_ref and n2
Instantiate an entity called "c" with the name C_comp
Set generic parameters for C_comp : C = 2E-12
Connect C_comp to n2 and electrically _ref
Instantiate an entity called "Inductor" with the name L_pkg
Set generic parameters for L_pkg : L = 1.01E-9
We connect L_pkg to n1 and n2
Instantiate an entity called "Resistor" with the name R_pkg
Set generic parameters for R_pkg : R = 32E-3
Connect R_pkg to P_in, and n1
Instantiate an entity called "Capacitor" with the name C_pkg
Set generic parameters for C_pkg : C = 0.13E-12
Connect C_pkg to P_in and electrical_ref
Instantiate an entity called "A2D_bit" with the name ADC
Set the generic parameters for the ADC: thres = 1.5
Connecting ADC to n2 and out

(iii) Modeling of Output Port

The physical model of the output port for NC7SZ157 was designed using VHDL-AMS, as shown in Alg. 3, based on the model parameters listed in Table 1.

Algorithm 3: Physical model of output port for NC7SZ157

We define the electrical terminals as VCC, P_in, P_out, n1, n2, and Do
Instantiate an entity called "MOSFET" with the name PMOS
Set generic parameters for PMOS : Vth = -0.6, B = -20, Kn = 0.01496, Va = -11.62, Abulk = 1.2
Connect the PMOS to P_in, n1, and VCC
Instantiate an entity called "MOSFET" with the name NMOS
We set the generic parameters for the NMOS: Vth = 0.5, B = 5.5, Kn = 0.02191, Va = 40.66, and Abulk = 1.2
The NMOS is connected to P_in, n1, and electrically _ref
Instantiate an entity called "Diode" with the name Diode1
Set generic parameters for Diode1 : Isat = 6.59E-11, R = 21, n = 2
Connect Diode1 to n1 and the VCC
Instantiate an entity called "Diode" with the name Diode2
Set generic parameters for Diode2 : Isat = 5.918E-14, R = 0.2158, n = 1.14
Connect Diode2 to the electrical_ref and n1
Instantiate an entity called "c" with the name C_comp
Set generic parameters for C_comp : C = 1.25E-12
Connect C_comp to n1 and electrically _ref
Instantiate an entity called "Inductor" with the name L_pkg
By setting the generic parameters for L_pkg: L = 0.91E-9
Connect L_pkg to n2 and P_out
Instantiate an entity called "Resistor" with the name R_pkg
Set generic parameters for R_pkg : R = 0.032
We connect R_pkg to n1 and n2
Instantiate an entity called "Capacitor" with the name C_pkg
Set generic parameters for C_pkg : C = 0.13E-12
Connect C_pkg to P_out and electrically _ref
Instantiate an entity called "VDC" with the name VDC2
Set generic parameters for VDC2 : DC = 3.3
Connect VDC2 to VCC and electrically _ref
Instantiate an entity called "D2A_bit" with the name DAC
Set generic parameters for DAC : para
The DAC is connected to Do and Pin_in

The functional area should be combined with the input and output port models to form a golden model of the component. Fig. 4(a) shows the simulation results of the golden model using the SystemVision software. The golden delay can be obtained from the component datasheet (the propagation delays I_0, I_1 and S to Z are 3.2 ns). The propagation delay is defined as the measurement starting when 50% of the rising or

falling edge of the input signal arrives and ending when 50% of the rising or falling edge of the output signal is reached, as shown in Fig. 4. The simulation parameters are as follows: the input *I0* is set to state '0, *I1* is set to state '1, the input clock is set to 50 MHz, and the output load is set to 1' kΩ. A comparison of the datasheet and simulation results confirms that the logic function of the developed model is accurate, and that the model is capable of reproducing the analog electrical characteristics of the port.

3. *Time Degradation Modeling*

To accurately simulate the impact of the TID on digital combinatorial and sequential logic, timing degradation must be considered, which can cause changes in circuit propagation delay and even disrupt the sequential logic function. As shown in Alg. 4, it is necessary to reconstruct the functional domain of the hybrid model and introduce a pin-to-pin signal propagation delay to model the propagation delay.

Algorithm 4: Timing degradation model of the functional area for NC7SZ157

1 If the value of signal *S* equals a high-level '1, then Check whether signal *I1* has changed (i.e., if it has had an event): The current value of *I1* is assigned to signal *Z* after a delay in *delay_I1*
2 If the signal *S* changes,then Assign the current value of *I1* to signal *Z* after a delay of *delay_s*
3 If neither *I1* nor *S* change,then The current value of *I1* is assigned to signal *Z*. End the if statement
4 If the value of the signal *S* equals the low level '0, then Check whether signal *I0* has changed (i.e., if it has had an event): The current value of *I0* is assigned to signal *Z* after a delay in *delay_I0*
5 If the signal *S* changes,then Assign the current value of *I0* to signal *Z* after a delay of *delay_s*
6 If neither *I0* nor *S* change,then The current value of *I0* is assigned to signal *Z*. End the if statement

In Algorithm 4, *delay_I1*, *delay_I0*, and *delay_s* are introduced as three parameters representing the pin-to-pin signal propagation delay from input ports *I1*, *I0*, and *S* to output port *Z*. The preradiation delay can be obtained from the component data. TID experiment results show that the propagation delay of NC7SZ157 in *S*-*Z* path is 3.2 ns at 0 krad(Si), 3.9 ns at 50 krad(Si) and 4.3 ns at 100 krad(Si). The simulation results are presented in Fig. 4(b).

From Fig. 4(b) it is clear that the signal transmission delay gradually increases as the TID increases. It can be concluded that the above model accurately represents the radiation-induced timing degradation of the component. Therefore, the proposed modeling method presented in this paper is feasible.

4. *Modeling TID Effect of Output Port*

The effect of the TID on the output port can be modeled by considering two key factors: the TID-induced effect on the

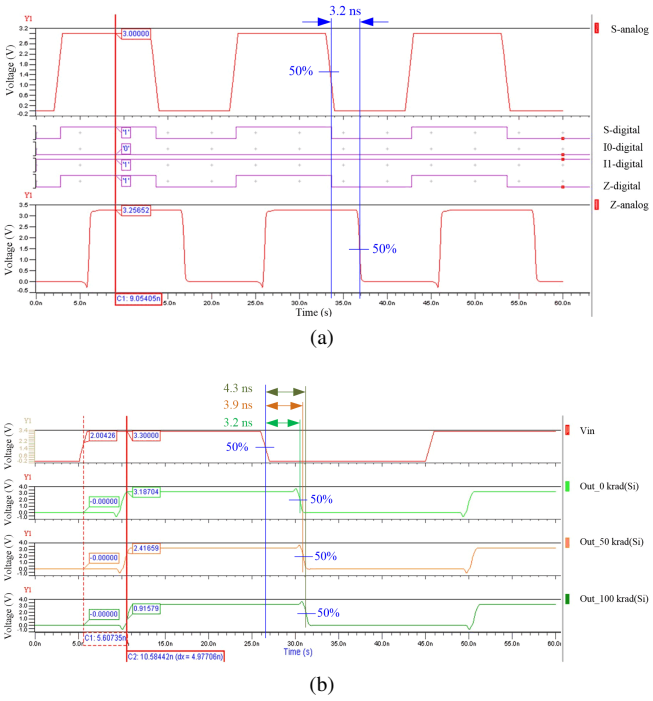


Fig. 4. Simulation results for NC7SZ157 of (a) Golden model; (b)Time degradation caused by TID effect.

threshold voltage and the carrier mobility of the port transistor, as described in the Introduction section of this chapter, on the effect of the TID on digital devices. To demonstrate the feasibility of this modeling approach, a CMOS output inverter circuit was constructed, as shown in Fig. 5(a), in the SystemVision simulation environment.

In Fig. 5(a) the load capacitance *C1* and resistance *R1* were as 2pF and 1 K Ω respectively. The simulation results are shown in Figs. 5(b) show that the electrical characteristics of the pull-up PMOS can be changed by adjusting the threshold voltage and carrier mobility. The conduction cases one–four reflect an increase in the threshold voltage of the PMOS and a decrease in the carrier mobility of the PMOS. It can be observed that, with an increase in the threshold voltage and a decrease in the carrier mobility of the pull-up PMOS, the PMOS on-resistance increases, leading to an increase in the rise time of the level at the output pin V_{out} and a decrease in the high-level amplitude. Therefore, the inclusion of the TID effect of the output pin threshold voltage of the transistor and carrier mobility in the model allows for the representation of the TID-related variation in the CMOS device port characteristics.

It is noteworthy that the four conduction cases shown in Fig. 5(b) are intended to verify the TID effect modeling method, in which the threshold voltage (V_{th}) and conductance parameters (k_n) are added to the port. During the modeling of the TID effect, the threshold voltage (V_{th}) and conductance parameter (k_n) of the device at different dose points were extracted by measuring the transfer characteristic curve of the transistor at the port of the TID experiment. Subsequently,

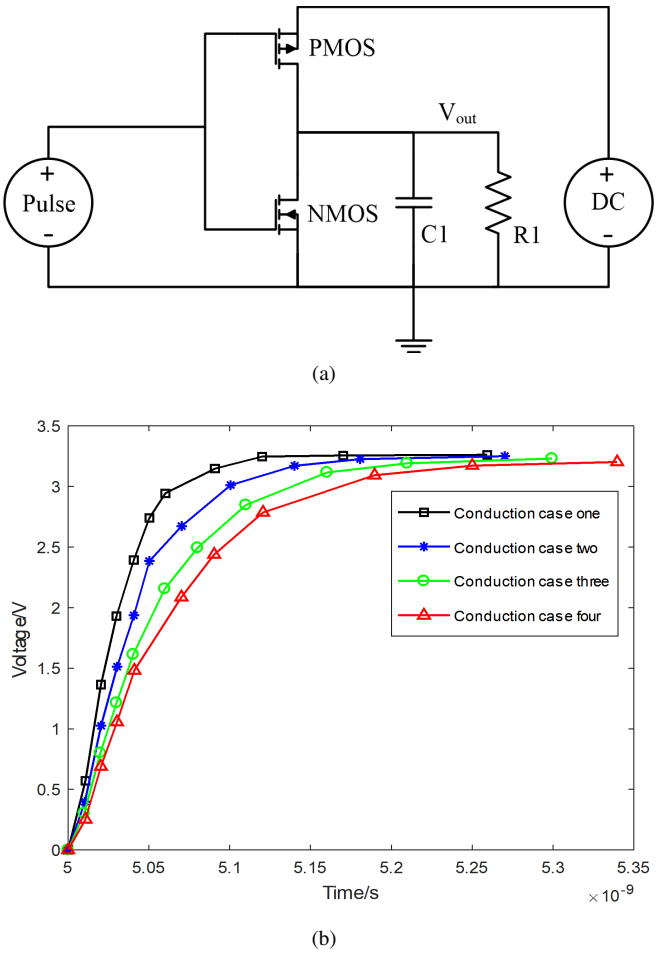


Fig. 5. Schematic of (a) inverter circuit for CMOS and (b) Simulation result of (a).

the extracted V_{th} and k_n are used as generic parameters for Alg. 3 to obtain simulation results for the TID effect at the port, as shown in Fig. 7.

III. EXPERIMENTS AND RESULTS

A. Experimental setup

To verify the TID effect modelling method for the CMOS digital IC proposed in this study, an experimental circuit for a CMOS non-inverting multiplexer, NC7SZ157, was set up. Subsequently, the TID experiment was conducted at the Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy of Sciences. The experimental board and the TID experimental environment are shown in Fig. 6. The experimental conditions are presented in Table 3.

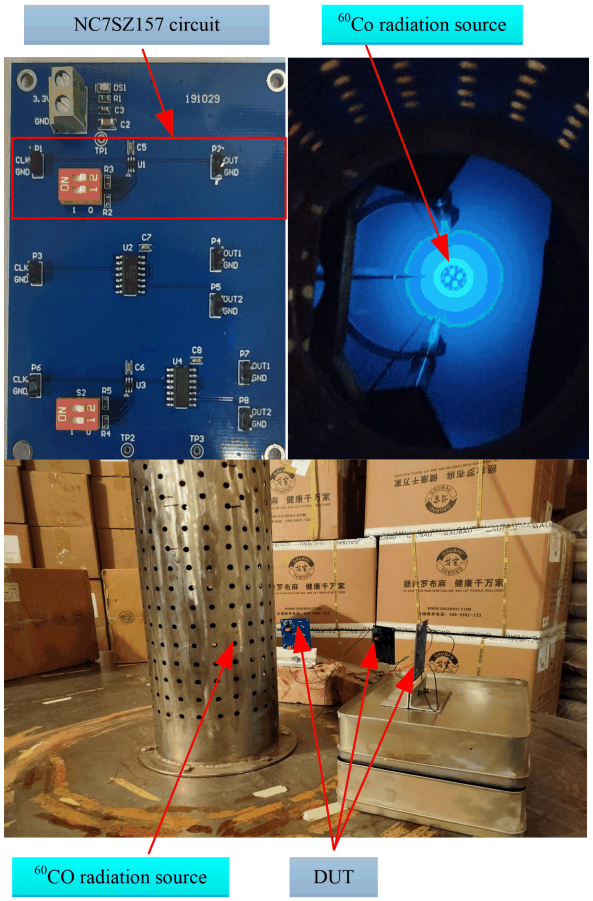


Fig. 6. TID Experiment platform

TABLE 3. TID Experiment Conditions.

Radiation conditions	Numerical value
Radiation source	^{60}Co
Radiation dose rate	50 rad(Si)/s
Total dose point	0 krad(Si),50 krad(Si),100 krad(Si)
Radiation method	Static no power,plus bias
Experiment equipment	MSO5104B mixed signal oscilloscope, Agilent 81104A signal generator, iTech IT6322 DC power
Experiment temperature	Room temperature 25°C

B. Results and Discussion

When measuring the experimental data, the *I0* pin of NC7SZ157 was set to '0, the *I1* pin was set to '1, and a 40 KHz square wave signal was applied to the *S* pin to measure the IBIS model and V-T waveform data of the output port *Z* at different dose points. The IBIS model primarily includes the V-I curves of the port diode and transistor, which are used to extract the characteristic parameters of the diode and transistor, and are substituted into Algs. 2 and 3 as generic parameters for the simulations. The V-T curve was compared with the simulation results, as shown in Fig. 7. It can be observed that the rise time t_r and fall time t_f of the simulation

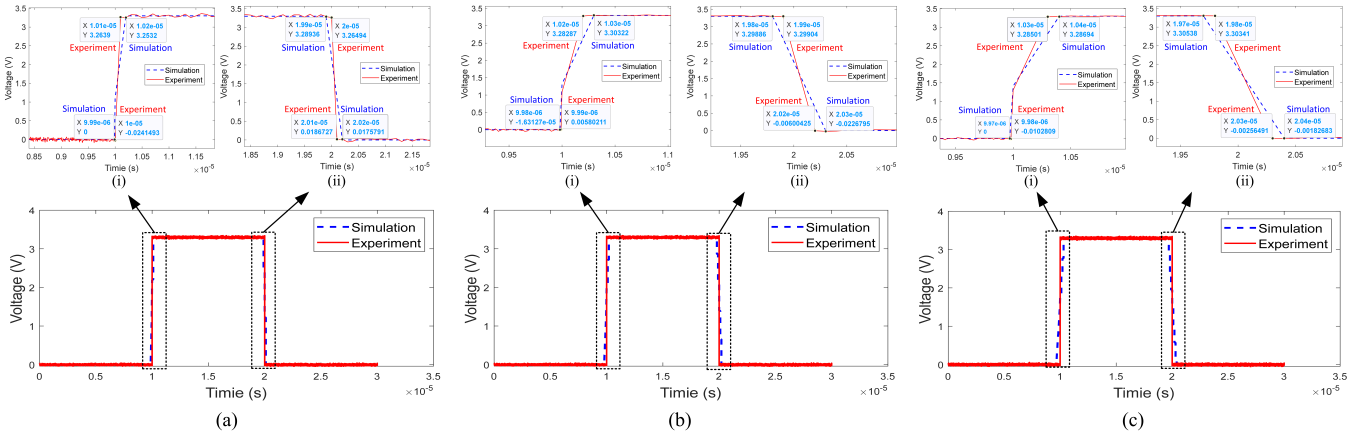


Fig. 7. Comparison of experiment results with simulation results at (a) 0 krad(Si); (b) 50 krad(Si) and (c) 100 krad(Si).

and experimental results increase with an increase in the TID. t_r and t_f refer to the times required for the output voltage of a component to change from 10% to 90% and from 90% to 10%, respectively.

The edge times of the experimental results are compared with those of the simulation results in Table 4. It can be seen that t_r and t_f increase with an increase in the TID. The relative error between the experimental and simulation results was calculated using the V-T data shown in Fig. 7. The relative error is defined as the average ratio of the difference between the experimental and simulation results to the experimental results for the voltage values within one period. The obtained relative errors were 0.2%, 0.6%, and 1.4% for dose points 0 krad(Si), 50 krad(Si), and 100 krad(Si), respectively. The results show that the model accurately reflects the effect of the TID on the CMOS digital IC termination. Table 4 also shows that the experimental results at 50 krad(Si) are close to the simulation results at 0 krad(Si) and that the experimental results at 100 krad(Si) are close to the simulation results at 50 krad(Si). This was because of the limited accuracy of the SystemVision simulation environment. In future studies, we aim to enhance the accuracy of the model and simulation to achieve a closer match between the simulation and experimental results. In addition, all the simulations were completed in less than 1 s, indicating the high efficiency of the model.

TABLE 4. Comparison of Simulation and Experiment Results.

Dose point	Edge	Experiments /ns	Simulation /ns
0 krad(Si)	t_r	80.2	177.0
	t_f	81.3	241.1
50 krad(Si)	t_r	179.1	265.0
	t_f	240.0	400.0
100 krad(Si)	t_r	266.7	353.8
	t_f	398.6	559.8

IV. CONCLUSION

This study proposes a three-phase TID effect modeling method for CMOS ICs based on the IBIS model to address the problems raised by transistor-level modeling when evaluating the TID effect in digital ICs. In the first phase, a gold model of a digital IC was developed. The transistor characteristic curves of the input and output buffers were first processed using the IBIS model of the component, and the physical parameters of the input and output ports were extracted using the diode and MOS physical equations. The VHDL language was used to model the functional areas of the components according to the truth table in the datasheet. The golden digital IC model was developed by combining the port and functional area models. In the second phase, the gold model is reconstructed based on the TID effect on the CMOS threshold voltage drift, carrier mobility degradation, and timing degradation effects to form the final TID effect model of the digital IC. In the third phase, the TID effect experiments were conducted using a CMOS non-inverting multiplexer, NC7SZ157, as an example. The 40 KHz waveform information of the NC7SZ157 output was measured at 0 krad(Si), 50 krad(Si) and 100 krad(Si), and the IBIS model was obtained to extract the feature parameters. The TID effect model was then loaded into the SystemVision environment for simulation. Finally, the simulation and experimental results were compared, which indicated that the relative error between the simulation and experimental results at each dose point was less than 2%. Thus, the feasibility and accuracy of the proposed modeling method were confirmed. The TID effect of other CMOS digital ICs can be simulated using this modeling method to evaluate their ability to tolerate the TID effect.

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